

Application No.: 10/826,342
Art Unit: 2624

Amendment under 37 CFR §1.111
Attorney Docket No.: 042336

REMARKS

Please reconsider the application in view of the foregoing amendments and following remarks.

Status of Claims

Claims 1-15 are pending in the present application. Claims 3, 6-8 and 10 are withdrawn from consideration. Claims 1, 2, 9 and 15 are herein amended. Applicant submits that no new matter has been added to the application by way of the above Amendment. Accordingly, the entry of the Amendment is respectfully requested.

Claim Rejections - 35 U.S.C. §112

The Examiner has rejected Claims 1-2, 4-5, 9, 11-15 rejected under 35 U.S.C. §112, second paragraph, as being indefinite because the limitation "the block to be resized in independent claims 1 and 15 have insufficient antecedent basis. Claims 1 and 15 have been amended. Applicant submits that amended claims 1 and 15 overcome the rejection and respectfully request that the rejection be withdrawn.

Claim Rejections - 35 U.S.C. §103

Claims 1-2, 4-5, 9 and 11-15 were rejected under 35 U.S.C. §103 (a) as being unpatentable over **Ke et al.** (US 6,094,226) in view of **Hideo et al.** (JP HI 1-053532 et al.). Applicants have amended the claims to patentably distinguish it from the cited references.

Independent claims 1 and 15

Claim 1, as amended, is drawn to ... *a line storage means including 1-line line memory having capacity for storing the image data corresponding to a lowest line of a resized block along the first direction of the image data outputted from the first resizing means*

Claim 15, as amended, is drawn to ... *a line storage section including 1-line line memory having capacity for storing the image data corresponding to a lowest line of a resized block along the first direction of the image data outputted from the first resizing circuit*

For example, as noted on page 12, second paragraph of the present specification, “Figs. 9A and 9B show the block sizes before and after the horizontal resizing processing in the present embodiment. Fig. 9A shows the block size outputted by the MPEG decoder 1, and Fig. 9B shows the block size to be outputted by the horizontal resizing circuit 2. While, as shown in Fig. 9A, 8×8 pixels are treated as one block at the MPEG decoder 1, **the block size is changed to 4×8**

pixels by the means of the resizing at the horizontal resizing circuit 2 as shown in Fig. 9B where the data of the lowest line thereof are stored to the line memory 3 as indicated."

On page 2 of the Office Action, the Examiner contends the following: "[a]pplicant argues that the line buffer of Ke does not have capacity corresponding to one line of the image data because it only stores the 5 MSB. The examiner disagrees the language of Ke states that "Yp may be stored in a line buffer as the 5 MSB" to reduce line storage requirements. This is only an option of reducing the storage requirements presented to someone implementing Ke which need not be exercised to practice the invention disclosed in Ke. Ke clearly implies that the larger memories could be used see (column 5 lines 50-55).

It is respectfully submitted that the Examiner is mis-characterizing the features of Ke. In column 5, lines 43-55, Ke discloses the following:

"[t]o reduce line storage requirements, yp may be stored in line buffer 232 as the 5 MSBs (most significant bits) of its original 8-bit value (e.g., line buffer of 5x640 bits), and yc may be the current 8-bit luma value. The 5-bit storage size for line buffer 232 provides enough precision to avoid introduction of artifacts into the resulting image, and is chosen to be 5 bits instead of 8 bits to reduce the silicon area required to implement this line buffer. (It is noted that the bit sizes, e.g. 5-bit value stored in line buffer

232 and the 8-bit current value, may be smaller or greater in other designs.)” (emphasis added)

In other words, to reduce line storage requirement in Ke, the line buffer 232 may accommodate 5×640 bits = 3200 pixel (1 bit per pixel) **instead of** 8×640 bits = 5120 pixels (1 bit per pixel).

In contrast, in the claimed invention, for example, only the data of the lowest line in the block are stored to the line memory 3. Since the number of pixels after the resizing in the horizontal direction is $(8 \times 720) = 5760$ pixels (see Fig. 9B), the line memory 3 only has to have a capacity capable of storing 1×720 pixels, that is, 720 pixels. **In other words**, even when the line storage requirement is reduced in Ke, it is still required to store more than one line of the image data, i.e., $(5 \times 640) = 3200$ pixels. **In contrast**, in the claimed invention, for example, the capacity of a line memory corresponds one line i.e., 1×720 pixels suffice. *see at least pages 11 and 12 of the present specification.*

As to the Examiner's contention that: "Ke clearly implies that the larger memories [or smaller memories] could be used see (column 5 lines 50-55)." Applicant submits that, unlike the claimed invention, Ke was not faced with the problem of reducing the line storage capacity. In fact, Ke explicitly acknowledges that its invention may not provide any space savings in column 6, lines 57-61 as follows:

“[] because line buffer storage is **not usually a problem** with horizontal scaling implementations, the conditional weighted average implementation of **the present invention may not provide any meaningful space savings on the silicon used for fabrication.**” (emphasis added)

Therefore, even if a person of ordinary skill in the art could combine elements of Ke with elements of Hideo for the motivation suggested by the examiner as obvious, the resulting combination will not be the claimed invention because neither Ke nor Hideo disclose or suggest at least *a line storage means including 1-line line memory having capacity for storing the image data corresponding to a lowest line of a resized block along the first direction of the image data outputted from the first resizing means* as recited in claims 1 and 15.

Given that neither Ke nor Hideo (alone or in combination) teach or disclose *a line storage means including 1-line line memory having capacity for storing the image data corresponding to a lowest line of a resized block along the first direction of the image data outputted from the first resizing means* in claim 1, Applicants submit that claims 1-2, 4-5, 9 and 11-15 are not obvious over these references and, accordingly, request that the rejection under 35 U.S.C. 103 be withdrawn.

Independent claims 1 and 15

Claim 1, as amended, also calls for ... *a second resizing means for resizing in a second direction intersecting said first direction by using the image data of the resized block to be resized, outputted from said first resizing means, and the image data of the lowest line of the resized block adjacent to the resized block to be resized, acquired from said line storage means.*

Claim 15 as amended, also calls for ... *a second resizing circuit for resizing in a second direction intersecting said first direction by using the image data of the resized block to be resized, outputted from said first resizing circuit, and the image data of the lowest line of the resized block adjacent to the resized block to be resized, acquired from said line storage section.*

As discussed above, because the combination of Ke and Hedio fail to disclose the line storage means, it necessarily fails to disclose a second resizing means as recited in claims 1 and 15 because the image data of the lowest line of the resized block adjacent to the resized block to be resized is acquired from the line storage means.

Therefore, it is further submitted that the above recited features of claims 1 and 15 are neither disclosed nor suggested by Ke and Hedio (alone or in combination). As such, the rejection is improper. Accordingly, it is requested that the rejection based on obviousness be withdrawn.

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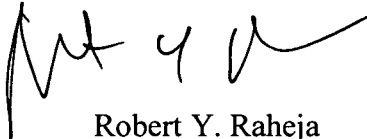
Conclusion

The Claims have been shown to be allowable over the prior art. Applicants believe that this paper is responsive to each and every ground of rejection cited in the Office Action dated November 12, 2008, and respectfully request favorable action in this application. The Examiner is invited to telephone the undersigned, applicants' attorney of record, to facilitate advancement of the present application.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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